A Fast-Locking, Sub-Threshold ADPLL Clock Synthesizer for Wireless Sensor Applications

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ABSTRACT

In this project, the design of an all-digital phase-locked loop (ADPLL) was implemented for use in a clock synthesizer for low-power applications. Digital implementations of the traditional analog PLL are becoming more popular due to the lower power consumption, smaller area, and noise immunity. Many implementations of APLLs are currently used for high-frequency RF applications consuming well into the mW of power and having an output frequency in the GHz range. The proposed PLL uses a low frequency reference of 65kHz and converts the frequency to 650kHz using an integer-N (N=10) PLL approach. The design consumes less than 5uW of power in 45nm running all circuits in the sub-threshold region and reduces the locking time to a maximum of 8 clock cycles by using a ring-oscillator based time-to-digital converter. The DCO has a LSB resolution of 692ps and an output frequency range from 540kHz to 1.2MHz. Portability was also a concern, and with the exception of the DCO, all other blocks can by synthesized.

1. INTRODUCTION

On a wireless sensor node, often the overhead of adding extra crystal oscillators to supply multiple clock domains is not feasible, but components such as the digital, analog and RF all require different clock frequencies. As the frequency of the crystal increases, the power tends to increase exponentially [8]. One approach is to use a low-frequency crystal that is already being used on the chip and increase its frequency through the use of a PLL. This higher frequency clock could be used to power analog portions of the chip or even used as a second fast clock for serial implementations of logic blocks that need to run multiple times in one period of the slow clock. Using an ADPLL is a compact, portable way to achieve this. Unlike a traditional analog PLL, an ADPLL assumes that all intermediate (control) signals are digital, but in many designs still contain analog components.

As integration and portability have become more important with CMOS process scaling, much emphasis has been placed on finding digital implementations of analog components in a PLL. The use of many analog components such as capacitors and inductors with high Qs requires intensive layout and need to be repeated every time the switch to a new technology occurs. It is desirable to be able to have HDL descriptions of all blocks in the system so that the circuit can be easily replicated in any technology using standard library cells. Also, by using all digital components, the immunity to supply noise and temperature variation is improved and it will result in a more compact implementation as the system can take advantage of scaled technology [9].

For wireless sensor networks, the power budget tends to be small (uW range) and if the high frequency clock needs to be duty cycled throughout the use of the chip, it's important that the lock time is fast to reduce power consumption during the frequency acquisition phase. Many systems use a binary search algorithm to determine the locking frequency as in [10], but this can take time depending on the number of delay stages in the circuit and the reference frequency. To reduce this, an algorithm based on the number of faster clock pulses between the two signals is used to make better guesses as to where the locking frequency will eventually fall.

The major block to be optimized is the DCO as it tends to consume 50-70% of the overall power budget [4]. The traditional oscillator in a PLL is a VCO controlled by an analog input voltage, but when going to a digital implementation, the control voltage becomes digital. As DCOs are a relatively new concept (many papers not found until late 90s or early 2000s), many focus on high performance RF applications and resort to using LC oscillators due to their low phase noise and high performance compared to ring oscillators. Since LC oscillators are not portable due to the layout of the inductor and capacitors, and the proposed design is not high-frequency, LC oscillators are not appropriate.

The paper is organized as followers: Section 2 describes the overall architecture for the system. Section 3 goes through each of the blocks within the system and their design. Section 4 describes the summary of the findings.

2. ADPLL ARCHITECTURE

Figure 1 shows the proposed ADPLL. It consists of a time-to-digital converter that replaces the phase-frequency detector and charge pump from the analog implementation, a DCO control logic block, the DCO, and the divider. Many implementations of proposed ADPLLs also have a digital loop filter used in the loop, but they also tend to use blocks from traditional PLLs such as charge pumps in conjunction with more digital blocks such as the TDC as in [4] and [11]. For this design, a loop filter is not needed since the output of the time-to-digital converter is simply a value from a counter and only occurs once for every pass through the loop. A filter in this context would not make sense and was eliminated from the design. This also helps to save area and power as most low-pass filter implementations require costly circuits such as multipliers and many registers for coefficient values.

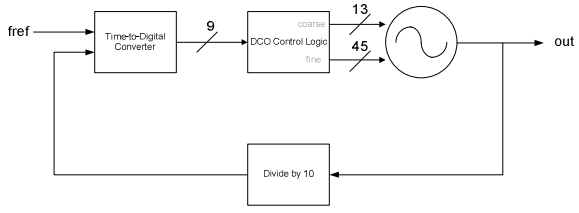

Figure 1. Proposed ADPLL Architecture

3. DESIGN COMPONENTS

3.1 Time-to-Digital Converter (TDC)

Before design for the TDC began, two topologies were investigated. The first, the Vernier delay technique, determines the reduced delay between the two signals by taking a difference of the delays. For this approach, a large range (of the full period) would require a large amount of area and stages to be accomplished. The second approach was an oscillator based approach that uses a fast oscillator to count the number of pulses that occur between the two signals. Using this approach, a large range can be achieved with compact area and the quantization error becomes scrambled across measurements. The proposed approach is not often seen in ADPLLs since the Vernier delay approach can be used for high-frequency applications, but was presented originally for PLL applications in [12].

Figure 2 shows the proposed TDC that uses a ring-oscillator based design that counts a certain number of pulses between the two clock input signals. Since it is a 9-bit counter, 512 clock pulses are needed to cover the span of a 1-period error (equivalent to a phase detector having a range of 2π). The period of the required fast clock needed to 24ns to achieve the desired resolution.

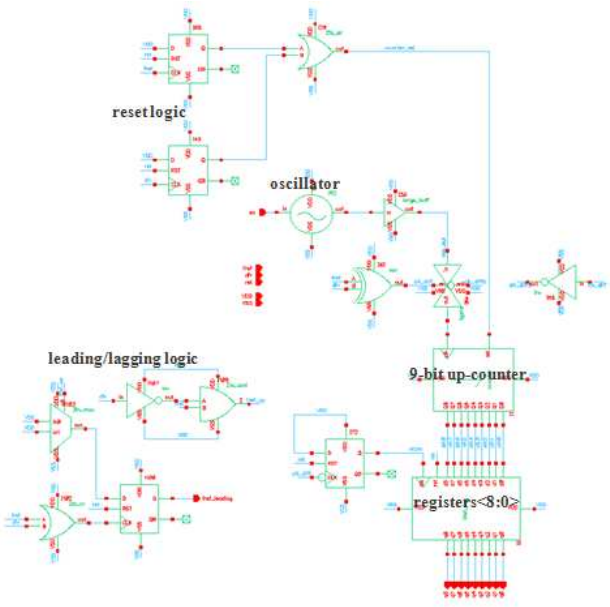

Figure 2. Time-to-digital converter schematic.

The expected results from the TDC circuit is that it will detect which signal has a rising edge first (output of the divider or the reference signal) and then start the fast VCO counter at that point. When the rising edge of the second signal occurs, the counter value is stored in a register bank and passed to the DCO control logic block. In the analog implementation, the PFD and charge pump would indicate through up and down currents whether or not the reference signal was leading or lagging. In the digital implementation, there is a bit that indicates if the reference is lagging and this helps determine whether or not the output frequency of the DCO should increase or decrease, respectively. Example simulation results for the case in which the reference frequency is leading are in Figure 3.

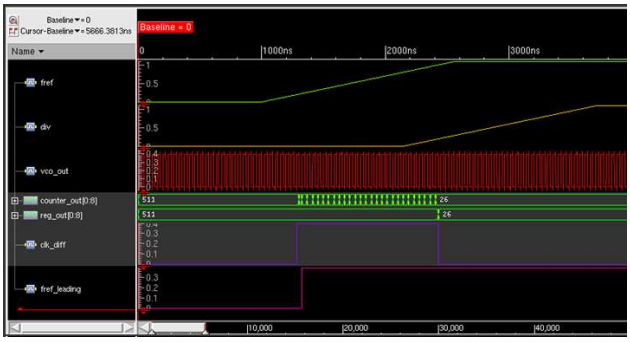

Figure 3. Time-to-digital converter simulation results for functionality.

The logic runs at 400mV and consumes 1.43µW running at the reference frequency of 65kHz.

3.2 DCO Control Logic Block

Most ADPLL logic blocks used to control the DCO use a binary search to determine the locking frequency as in [10]. Although this algorithm is O(lgn) and relatively fast, there are still improvements that can be made. Using the ring-oscillator based TDC, the number of pulses can indicate how different the reference and the division pulses are from each other. If the number is very small, then the initial guess of midway through the frequency range of the DCO is correct, else the search for the correct frequency should not start in the center. This is the strategy taken in the control logic block.

The coarse stage is used to determine which larger region of the frequency range to begin the fine tuning. The output of the logic block to the coarse stage is a one-hot 45 bit output. The number of outputs bits sounds high due to the low frequency: many delay stages are needed to cover one full period of the input clock. The coarse stage breaks this up into 6 separate sections. Within the fine stage, the initial guess is in the center of the chosen section from the coarse stage. After this, the one-hot bit gets shifted either to the left or the right depending on whether the reference is leading or lagging. This leads to a maximum of 8 steps to lock. Once it has locked, there are outputs to control the headers of the delay cells in the DCO. If any delay cells are not being used, they are power gated to reduce the power consumption. This block was used as a functional block completed in HDL with the emphasis being an algorithm that can be used in conjunction with the TDC to reduce the number of cycles to lock.

3.3 Digitally Controlled Oscillator (DCO)

The DCO uses a ring-oscillator topology since LC based oscillators tend to be used for RF applications due to their ability to achieve high frequencies and low phase-noise. Also, since portability is a focus of the ADPLL, using inductors and completing the layout would take time and need to be redone in the event a new technology was used.

Most DCO circuits tend to have multiple tuning stages, where each has delay cells of different delay time. The signal will begin by going through a coarse-delay stage that determines what subset of the overall tuning range of the DCO that it needs to lock to. It then uses a finer stage to more finely tune that frequency within the subset of the overall frequency. This tends to eliminate the

number of cycles it takes to lock by quickly determining which "sets" of the tuning range do not need to be searched. For this design, a fine and coarse tuning stage are used.

Before the DCO was built, different delay cell topologies were surveyed from the literature and simulated to determine their delay to power performance. Four delay cells were encountered most frequently in ring-oscillators and are the inverter, the shunt capacitor inverter, the hysteresis delay cell (HDC), and the current starved inverted.

3.3.1.1 Delay Cells

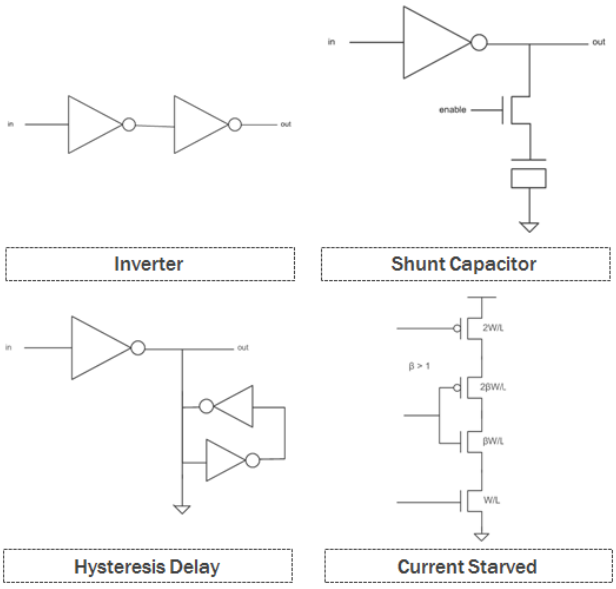

Figure 4. Delay cell topologies surveyed.

Considering the fact that hysteresis delay cells require ratioed logic that tends to not be reliable in the sub-threshold regime, they were initially not a feasible choice. Current starved can be made extremely low-power, but require a current reference circuit, proper sizing, and an analog control voltage. To determine which delay cell to use, a sweep of the output frequency and average power consumed per period was found for each of the delay cell topologies in Figure 5.

It can be seen that the HDC can get very small delays (high frequencies), but at the penalty of a high power consumption. Since the application space I am looking at is for low-frequency, low-power applications, the HDC was immediately discounted. Looking at the curve for the inverter, it can be seen that it can achieve very high frequencies for a small amount of power. This delay cell was used for the fine tuning stage. Although the current starved topology can achieve very high delays, it seems to consume more power and requires a current reference that would require an analog control voltage. The shunt capacitor inverter was used for the coarse stage due to its relatively high delay and low power consumption.

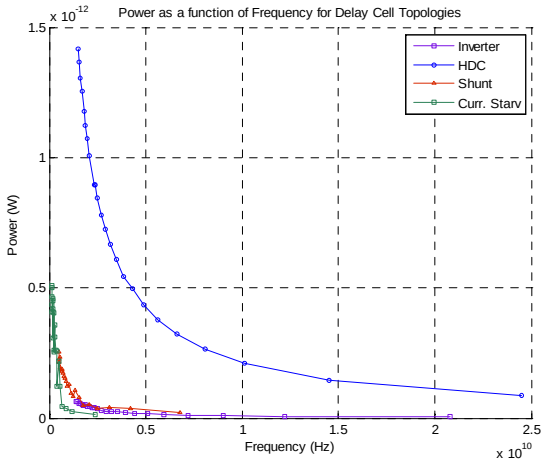

Figure 5. Delay cell power versus frequency curves at 1.1 V.

3.3.1.2 Implementation

The schematic in Figure 6 consists of the coarse stage block followed by the fine stage block. The sets of transmission gates are used since the logic block for the DCO outputs a one-hot encoded set of control signals for each block and only has one transmission gate active at any time. A feature of both the fine and coarse stage blocks is that the unused delay cells are power gated once the APLL is in lock. The logic block disables portions of the delay cell unless they need to be turned on to re-calibrate.

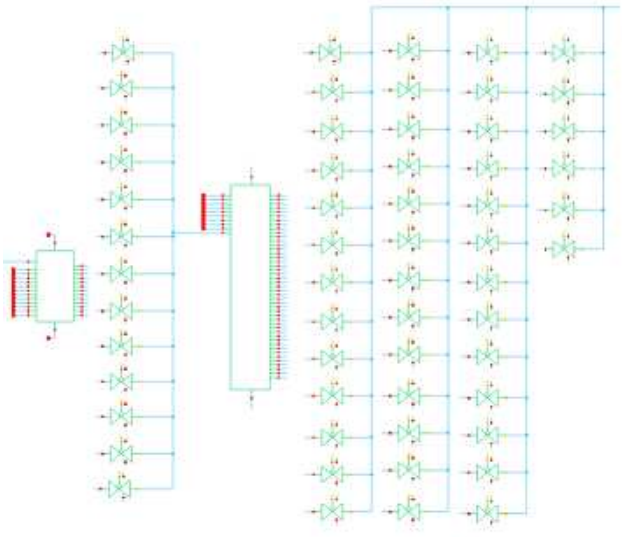

Figure 6. Digitally Controlled Oscillator schematic.

The DCO was tested for a few sets of input bits (smallest, mid, largest) to determine a linear operating range. The mid-output frequency is 650kHz and is linear for ±150kHz. To show functionality of the block, the mid-range output is shown in Figure 7.

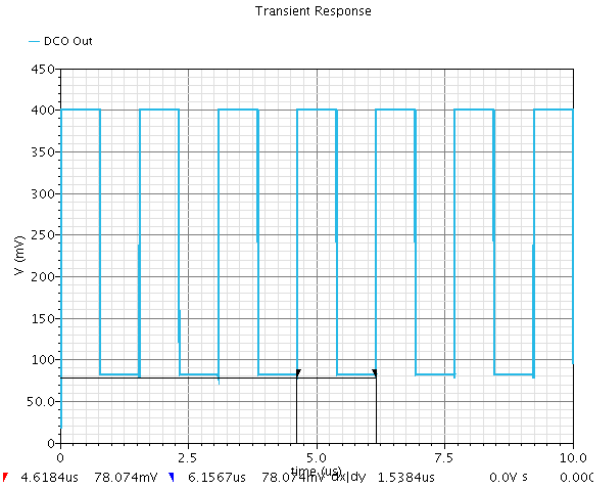

Figure 7. Digitally Controlled Oscillator output frequency when both fine and coarse tuning stages are tuned to the mid-values.

Although it was difficult to find low-frequency or sub-threshold DCOs in the literature, the following works were the most similar. As can be seen, the presented DCO consumes the least amount of power, but for a smaller operating frequency. Here, all of the delay cells are active, but power consumption can be further reduced by power gating the unused delay cells using the enable signals on each block. Assuming the output frequency falls around the middle range of the DCO, 50% of power for the delay cells should be saved.

Work	Power	Op. Freq	Voltage
[1]	5.4uW	3.4MHz	1 V
[2]	5.2uw	3.89MHz	1 V
[3]	140uW	200MHz	1 V
[4]	110uW	200MhZ	0.8 V
[5]	75.9uW	239MHz	1 V
[6]	340uW	450MHz	1.8 V
This Work	935nW	650kHz	0.4V

Table 1. Compared works for the DCO.

4. SUMMARY

Presented was a fast-locking, sub-threshold ADPLL architecture used for low-power clock synthesis applications. Focus was put into the design of the DCO as it tends to consume a majority of the system power. Due to the fast clock within the TDC, it consumed similar power consumption to the DCO. Although the final simulation results are not presented here for the system, the logic and architecture behind the ADPLL should be functional and consume less than 5uW @ 650kHz with all blocks operating in the sub-threshold region at 400mV for a worst-case power consumption (all blocks are on).

5. ACKNOWLEDGMENTS

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